

REMARKS/ARGUMENTS

Claims 44, 48, 49 and 60 to 68 are in the application, of which claims 44, 61 and 65 are the independent claims. Claims 44, 48, 61, 62, 65 and 66 are amended herein. No claims have been newly canceled herein. No new claim are added herein. Reconsideration and further examination are respectfully requested.

No new matter is believed to be added by the claim amendments herein. Reconsideration and further examination are respectfully requested.

Claim Rejections – 35 USC § 103

Claims 44, 48, 49 and 60 to 68 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over U. S. Pat. No. 6,476,499 (“Hikita”) and JP405123237A (“Shimizu”). Claims 48, 49 and 60 to 68 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over Hikita, Shimizu and the Flip Chip Ball Grid Array (FPBGA) Package Family reference (“Flip Chip”). Claims 44, 48, 49, 60, 62-64 and 66 to 68 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over U.S. Pat. No. 5,894,172 (“Hyozo”), Shimizu and Flip Chip. Claims 44, 48, 49 and 60 to 68 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over Hikita and JP362169448A (“Hiromasa”). Claims 48, 49 and 60 to 68 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over Hikita, Hiromasa and Flip Chip. Claims 44, 48, 49, 60, 62 to 64 and 66 to 68 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over Hyozo, Hiromasa and Flip Chip. Claims 65 to 68 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over Hikita, Hiromasa and Shimizu. Claims 65 to 68 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over Hikita, Hiromasa, Flip Chip and Shimizu. Claims 65 to 68 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over Hyozo, Hiromasa, Flip Chip and Shimizu. Reconsideration and withdrawal of these rejections are respectfully requested.

Independent Claim 44 is directed to a circuit component comprising a substrate and a semiconductor chip over a top surface of said substrate. The semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface. The semiconductor chip comprises multiple pads at said front surface. An identity of product is

directly on said back surface of said semiconductor chip. Multiple metal bumps are between said multiple pads of said semiconductor chip and said top surface of said substrate. An optically transparent layer is vertically over said identity of product. The identity of product is visible through said optically transparent layer.

Independent Claim 61 relates to a circuit component comprising a substrate and a semiconductor chip over a top surface of said substrate. The semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface. The semiconductor chip comprises multiple pads at said front surface. An identity of manufacturer is directly on said back surface of said semiconductor chip. Multiple metal bumps are between said multiple pads of said semiconductor chip and said top surface of said substrate. An optically transparent layer vertically over said identity of manufacturer, wherein said identity of manufacturer is visible through said optically transparent layer.

Independent Claim 65 is directed to a circuit component comprising a substrate and a semiconductor chip over a top surface of said substrate. The semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface. The semiconductor chip comprises multiple pads at said front surface. A bar code is directly on said back surface of said semiconductor chip. Multiple metal bumps are between said multiple pads of said semiconductor chip and said top surface of said substrate. An optically transparent layer vertically over said bar code. The bar code is visible through said optically transparent layer.

The applied references, either alone or in combination, are not seen to teach or suggest the foregoing combination of features of each of independent Claims 44, 61 and 65.

The Examiner considers that “it would have been obvious to one of ordinary skill in the art to combine the teachings of Hikita et al. with those of Shimizu.” Office Action, page 3, lines 18-19. Applicants respectfully disagree.

Hikita’s invention is related to the technology field of a semiconductor chip package. *See, e.g.,* Hikita, title and col. 1, lines 12 to 16. One of ordinary skill in the art at the time the present invention was made would have molded a chip in a chip package to prevent the chip from

being detected in a final product. For example, Hikita teaches that “[t]he chip-on-chip semiconductor device is molded and then delivered to the market and, when a need arises to check makers and the like of the respective semiconductor chips incorporated in the semiconductor device, the back faces of the semiconductor chips are exposed from a mold package for checking the specific informational notations of the semiconductor chips. Thus, production information on the semiconductor chips can be checked.” *See*, Hikita, col. 8, lines 22-30. There is not seen to be any teaching or suggestion in Hikita that an identity of product or manufacture or a bar code directly on a back surface of a semiconductor chip can be visible in a final product delivered to the market. Only in certain cases is the back face of Hikita’s semiconductor chip exposed from a mold package to allow a check of the production information. As a result, there is not motivation of having the claimed optically transparent layer to be applied to Hikita’s device.

Even though Shimizu teaches that a bar code printed on a tableware can be printed with a transparent resin member, Shimizu’s technical field is related to tableware, but not related to a chip package. The design considerations of processing a chip package are significantly different from those of processing a tableware because a tableware is typically viewed in a final product, but a semiconductor chip is typically molded and not visible in a final product.

Because the design considerations of Hikita and Shimizu are significantly different, one of ordinary skill in the art would not consider or would not be motivated to combine the subject matter that Hikita’s identity of product and manufacturer or Hikita’s bar code shown in Fig. 15 or 16A directly on a back surface 24 of Hikita’s chip 2 is printed with Shimizu’s transparent resin member.

Accordingly, Applicants submit that one skilled in the art would not consider or be motivated to combine the teachings of Hikita and Shimizu in the manner suggested in the Office Action to arrive at the combination of features of Claims 44, 61 and 65. In this regard, none of the other prior art references are seen to remedy the above-discussed deficiencies of Hikita and Shimizu.

Furthermore, the Examiner considers that Hiromasa teaches a transparent resin through which identification information can be read. *See*, Office Action, page 8, lines 3 and 4. Hiromasa

teaches that an identity of product is printed on a bottom of a recessed part 3 in Hiromasa's package material 2. However, there is not seen to be any teaching or suggestion in Hiromasa regarding printing identification information on Hiromasa's chip 7 molded by Hiromasa's package material 2. Hiromasa's chip 7 is believed not to be visible in a final product because Hiromasa's package material 2 is not taught to be transparent. In this regard, even if Hiromasa's chip 7 could be replaced with Hikita's chip with an identity of product or manufacture and a bar code printed directly thereon, the identity of product or manufacture and a bar code are not believed to be visible because Hiromasa's package material 2 is not taught to be transparent.

The other applied references, Flip Chip and Hyozo, are not seen to cure the above-discussed deficiencies of Hikita, Shimizu and Hiromasa.

For the reasons discussed above, Claims 44, 61 and 65 are believed to be allowable over the applied references. Accordingly, reconsideration and withdrawal of the rejections of Claims 44, 61 and 65 are respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the remarks set forth herein, Applicant submits that the claims are now in condition for allowance and respectfully requests a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

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